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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,491	06/20/2003	Frank Sacca	0120104C	9887

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FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
SWERDLOW, DANIEL	
ART UNIT	**PAPER NUMBER**
2646	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,491	SACCA ET AL.	
	Examiner	Art Unit	
	Daniel Swerdlow	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-22,24,25,27-30 and 32-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-22,24,25,27-30 and 32-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3 June 2005 has been entered.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. **Claims 33 through 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiyoshi (US Patent 5,734,703).**

4. Regarding Claim 33, Hiyoshi discloses a circuit for connecting a modem to a two-wire circuit (i.e., a telephone line) (Fig. 9, reference 540, 103; column 1, lines 16-20) comprising: modem output driver (i.e., DC loop current) circuit (Fig. 9, reference 520: column 18, lines 3-4) having an operational amplifier (i.e., a first operational amplifier) with a feedback path from the transistor emitter to the inverting input of the amplifier (i.e., configured to linearly vary a line current of the telephone line) having an output connected to the base of a transistor (i.e., a first electronic inductor transistor) connected across a rectified (Fig. 9, reference 103; column 18, line 5) two-wire circuit (i.e., tip and ring voltage of the telephone line) and a semiconductor inductor circuit (Fig. 9, reference 540; column 18, lines 3-4) (i.e., AC current circuit) having another

operational amplifier (i.e., a second operational amplifier) having an output connected to the base of a transistor (i.e., a second electronic inductor transistor) connected across a rectified (Fig. 9, reference 103; column 18, line 5) two-wire circuit (i.e., tip and ring voltage of the telephone line). While Claim 33 has been amended by applicant to recite that an emitter of the second electronic inductor transistor is coupled to ground, it was well-known to one skilled in the art that the selection of ground is an arbitrary convention. As such the recitation carries no patentable weight.

5. Regarding Claim 34, Hiyoshi further discloses a voltage divider comprising two resistors connected to the positive input of the operational amplifier in the modem output driver (i.e., DC loop current) circuit (i.e., the first operational amplifier) (Fig. 9, reference 520).

6. Regarding Claim 35, Hiyoshi further discloses resistors connected to the emitter of the transistor in the modem output driver (i.e., DC loop current) circuit (i.e., the first electronic inductor transistor) (Fig. 9, reference 520).

7. Regarding Claim 36, Hiyoshi further discloses the operational amplifier in the semiconductor inductor circuit (i.e., AC current circuit) (Fig. 9, reference 540) (i.e., the second operational amplifier) having a positive input connected to a modem output driver (i.e., a transmit signal driver of the modem) (Fig. 9, reference 520; column 18, lines 3-4).

8. Regarding Claim 37, Hiyoshi further discloses a balancing bridge (i.e., impedance matching) circuit (Fig. 9, reference 11; column 9, lines 52-55) connected between the positive input of the operational amplifier in the semiconductor inductor circuit (i.e., AC current circuit) (Fig. 9, reference 540) (i.e., the second operational amplifier) and the collector of the transistor in

the semiconductor inductor circuit (i.e., AC current circuit) (i.e., the second electronic inductor transistor).

Claim Rejections - 35 USC § 103

9. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

10. **Claims 18 through 22, 24, 25, 27 through 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiyoshi in view of Gay et al. (US Patent 4,796,295).**

11. Regarding Claim 18, Hiyoshi discloses a circuit for connecting a modem to a two-wire circuit (i.e., a telephone line) (Fig. 9, reference 540, 103; column 1, lines 16-20) comprising: a voltage controlled current source including an operational amplifier (Fig. 9, reference 540) having a positive input connected to a modem output driver (i.e., a transmit signal driver of the modem) (Fig. 9, reference 520; column 18, lines 3-4) with a feedback path from the transistor emitter to the inverting input of the amplifier (i.e., configured to linearly vary a line current of the telephone line); the operational amplifier having an output driving the base of a transistor to form a semiconductor inductor circuit (i.e., an electronic inductor transistor) (Fig. 9, reference 540; column 18, lines 3-4); the transistor connected across a rectified (Fig. 9, reference 103; column 18, line 5) two-wire circuit (i.e., tip and ring voltage of the telephone line). Therefore, Hiyoshi anticipates all elements except a second transistor having a base connected to the collector of the electronic inductor transistor. Gay discloses a telephone interface circuit (Fig. 1) with a transistor (Fig. 1, reference 6) connected to the output of an operational amplifier (Fig. 1, reference 14) driven by an amplifier (Fig. 1, reference 18) that receives a transmit signal (Fig. 1,

reference 20; column 3, lines 35-39). As such, the transistor (Fig. 1, reference 6) corresponds to the transistor in Hiyoshi, Fig. 9, reference 540 and to the electronic inductor transistor claimed. Gay further discloses another transistor (Fig. 1, reference 5) with a base connected to the collector of the first (i.e., electronic inductor) transistor. Gay discloses that by driving the second transistor in this way, line current is not drawn until the first (i.e., electronic inductor) transistor is active (column 4, lines 9-16). This avoids leakage currents that could result in the telephone line spuriously going into an off-hook state, especially when plural devices share a line. Therefore it would have been obvious to one skilled in the art at the time of the invention to apply the second transistor with a base connected to the collector of the first transistor as taught by Gay to the circuit taught by Hiyoshi for the purpose of reducing leakage currents and their undesirable effects.

12. Regarding Claim 19, Hiyoshi further discloses the negative input of the operational amplifier connected, via a resistor, to the transistor emitter (Fig. 9, reference 540).

13. Regarding Claim 20, Hiyoshi further discloses a resistor and capacitor forming a voltage divider connected to the positive input of the operational amplifier (Fig. 9, reference 540).

14. Regarding Claim 21, Hiyoshi further discloses a balancing bridge (i.e., impedance matching) circuit (Fig. 9, reference 11; column 9, lines 52-55) connected between the positive input of the operational amplifier and the collector of the transistor (Fig. 9, reference 540).

15. Regarding Claim 22, Hiyoshi further discloses a resistor connected between the operational amplifier positive input and the transistor emitter (i.e., to an emitter of the electronic inductor transistor) (Fig. 9, reference 540).

16. Regarding Claim 24, Hiyoshi further discloses a capacitor between the modem output driver (i.e., a transmit signal driver) and the positive input of the operational amplifier (Fig. 9, reference 520, 540).

17. Regarding Claim 25, Hiyoshi discloses a circuit for connecting a modem to a two-wire circuit (i.e., a telephone line) (Fig. 9, reference 540, 103; column 1, lines 16-20) comprising: an operational amplifier (Fig. 9, reference 540) having an output driving the base of a transistor to form a semiconductor inductor circuit (i.e., an electronic inductor transistor) (Fig. 9, reference 540; column 18, lines 3-4); a hookswitch (Fig. 9, reference 550) connected between the two-wire circuit and the rectifier (Fig. 9, reference 103) and therefore, not connected between the rectified tip and ring voltage and the modem; and a modem output driver (Fig. 9, reference 520; column 18, lines 3-4) with a feedback path from the transistor emitter to the inverting input of the amplifier (i.e., configured to linearly vary a line current of the telephone line). Therefore, Hiyoshi anticipates all elements except a second transistor having a base connected to the collector of the electronic inductor transistor. Gay discloses a telephone interface circuit (Fig. 1) with a transistor (Fig. 1, reference 6) connected to the output of an operational amplifier (Fig. 1, reference 14) driven by an amplifier (Fig. 1, reference 18) that receives a transmit signal (Fig. 1, reference 20; column 3, lines 35-39). As such, the transistor (Fig. 1, reference 6) corresponds to the transistor in Hiyoshi, Fig. 9, reference 540 and to the electronic inductor transistor claimed. Gay further discloses another transistor (Fig. 1, reference 5) with a base connected to the collector of the first (i.e., electronic inductor) transistor. Gay discloses that by driving the second transistor in this way, line current is not drawn until the first (i.e., electronic inductor) transistor is active (column 4, lines 9-16). This avoids leakage currents that could result in the telephone

line spuriously going into an off-hook state, especially when plural devices share a line. Therefore it would have been obvious to one skilled in the art at the time of the invention to apply the second transistor with a base connected to the collector of the first transistor as taught by Gay to the circuit taught by Hiyoshi for the purpose of reducing leakage currents and their undesirable effects.

18. Regarding Claim 27, Hiyoshi further discloses the negative input of the operational amplifier connected, via a resistor, to the transistor emitter (Fig. 9, reference 540).

19. Regarding Claim 28, Hiyoshi further discloses a resistor and capacitor forming a voltage divider connected to the positive input of the operational amplifier (Fig. 9, reference 540).

20. Regarding Claim 29, Hiyoshi further discloses a balancing bridge (i.e., impedance matching) circuit (Fig. 9, reference 11; column 9, lines 52-55) connected between the positive input of the operational amplifier and the collector of the transistor (Fig. 9, reference 540).

21. Regarding Claim 30, Hiyoshi further discloses a resistor connected between the operational amplifier positive input and the transistor emitter (i.e., to an emitter of the electronic inductor transistor) (Fig. 9, reference 540).

22. Regarding Claim 32, Hiyoshi further discloses a capacitor between the modem output driver (i.e., a transmit signal driver) and the positive input of the operational amplifier (Fig. 9, reference 520, 540).

Response to Arguments

23. Applicant's arguments filed 3 June 2005 have been fully considered but they are not persuasive. In the paragraph spanning pages 10 and 11 of the response, applicant alleges that

Hiyoshi provides no motivation for including the second transistor. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, one of ordinary skill in the art would have recognized that the second transistor avoids leakage currents that could result in the telephone line spuriously going into an off-hook state, especially when plural devices share a line. In the same paragraph, applicant alleges that the use of photo-couplers in Hiyoshi obviates the need for additional isolation. Examiner respectfully disagrees. The photo-couplers in Hiyoshi isolate modem circuitry from the telephone line. As stated above, the motivation for enhanced isolation is to prevent excessive loop current that could cause the telephone line spuriously going into an off-hook state.

24. Examiner notes for the record that similar transistor configurations are disclosed, for example, in US Patent 5,606,598 to Karnowski et al. (Fig. 5, reference 121, 122), US Patent 5,220,597 to Horiuchi (Fig. 7, reference 70, 71), US Patent 4,794,640 to Yeh (Fig. 3, reference Q1, Q2) and US Patent 5,608,795 to Gay (Fig. 1, reference Q1, Q2).

25. In the first complete paragraph on page 12 of the response, applicant alleges that the recitation of an emitter of the second electronic inductor transistor being coupled to ground patentably distinguishes the claim from Hiyoshi. Examiner respectfully disagrees. As stated in

the prior art rejection above, it was well-known to one skilled in the art that the selection of ground is an arbitrary convention. As such the recitation carries no patentable weight.

26. On page 13 of the response, applicant makes arguments relating to Claims 23 and 31. These claims having been cancelled by applicant, the arguments are moot.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Swerdlow whose telephone number is 571-272-7531. The examiner can normally be reached on Monday through Friday between 7:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh H. Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel Swerdlow
Examiner
Art Unit 2646

ds
2 August 2005